

PLC 220 Hands-On Assessment Module 3

Student Name:	 N#	Date:	

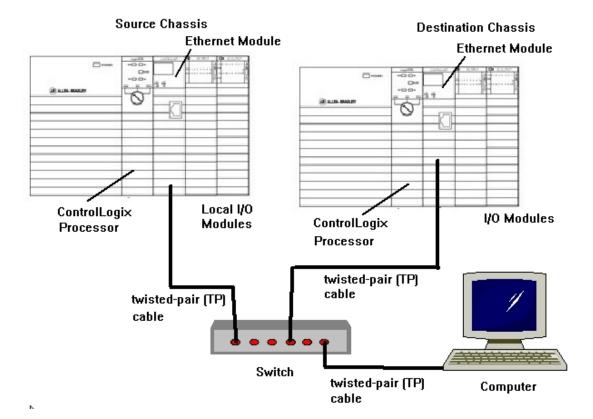
This hands-on assessment requires that each student successfully demonstrates each of these tasks to the instructor's satisfaction. There is no grade for this assessment.

Prior to taking this assessment, the student must pass (minimum of 80%) the Knowledge and Application Assessment.

The student cannot proceed to the HOA for the next module without completing this HOA

Equipment Required:

- ControlLogix Demo with processor Source / Produced Chassis
- ControlLogix Demo with processor-Destination / Consumed Chassis
- Twisted pair cables
- Computer with Studio 5000, BOOTP/DHCP Server and RSLinx software
- Ethernet Switch



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Figure 1-A. Source and destination controller connected by Ethernet. Set-up hardware as shown in Figure 1-A

 Determine the following computer information IP Address:
Subnet Mask:
Ethernet Address:
 Set the Ethernet module in the Source / Produced Chassis to default setting. Using the BOOTP/DHCP Server assign an IP Address and Subnet Mask
that will work on the same network as the computer to the Ethernet Module.
Record the following Ethernet Module information
IP Address:
Subnet Mask: Ethernet Address:
Ethernet Address.
Configure the Ethernet Module to Static Set-up
 3. Set the Ethernet module in the Destination / Consumed Chassis to default setting.
Using the BOOTP/DHCP Chassis Server assign an IP Address and Subnet
Mask that will work on the same network as the computer to the Ethernet Module.
Record the following Ethernet Module information
IP Address:
Subnet Mask:
Ethernet Address:
Configure the Ethernet Module to Static Set-up
 4. Verify connections using PING utility
 5. Using Studio 5000 software develop a Project Files for the processor in the Source / Produced Chassis that will:

- Name the Processor in the Source / Produced Chassis as ONE
- Name the Processor in the Destination / Consumed Chassis as TWO



- Name the Ethernet Module in the Source / Produced Chassis as ONE Enet
- Name the Ethernet Module in the Destination / Consumed Chassis as TWO Enet
- Name the I/O Modules based on their slot location, i.e. Slot 2, etc.
- Configure a recycling 10 second Timer in Processor ONE that will RUN when the SS7 is TRUE / ON
- Create a tag Recycle Timer for the Timer instruction
- Create a DINT tag named ONE_Tag1
- Move the ACC value of Recycle Timer to ONE Tag1 tag MOV Instruction
- Configure a MESSAGE Instruction to will send the value of ONE_Tag1 to a tag called TWO Tag1 located in Processor TWO.
- Create Mess1 for MESAAGE Instruction control tag
- The MESSAGE instruction will continually send the ONE_Tag1value to Processor TWO when SS4 switch on Processor ONE board is TRUE / ON
- Create a second MOV instruction that will move the ACC value of Recycle_Timer to a tag named Produced_Tag1
- Create a DINT tag named Produced Tag1
- Configure Produced Tag1 as a Produced Tag with 5 connections
- Save the Project File as Processor ONE.ACD

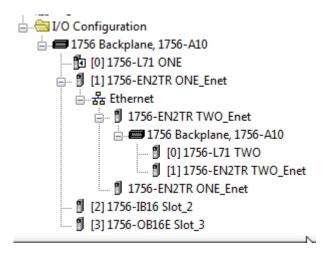


Figure 2 - A I/O Configuration Processor ONE



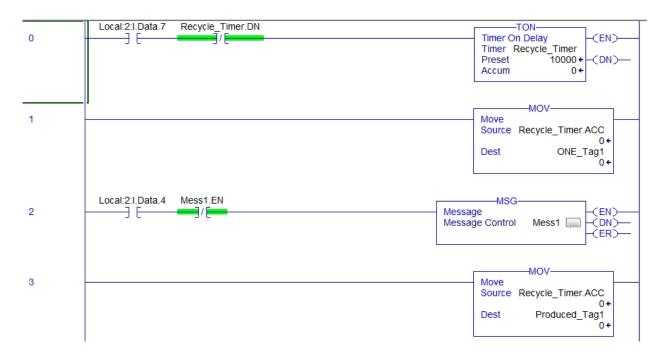


Figure 3 – A Ladder Logic Processor ONE

- _ 6. Using Studio 5000 software develop a Project Files for the processor in the Destination / Consumed Chassis that will:
 - Name the Processor in the Destination / Consumed Chassis as TWO
 - Name the Processor in the Source / Produced Chassis as ONE
 - Name the Ethernet Module in the Source / Produced Chassis as ONE Enet
 - Name the Ethernet Module in the Destination / Consumed Chassis as TWO_Enet
 - Name the I/O Modules based on their slot location, i.e. Slot 2, etc.
 - Create a tag named TWO_Tag1 that will show the value of ONE_Tag1 from processor ONE
 - Create a Consumed tag named Consumed_Tag1 that will get its value from the Produced Tag1 tag in Processor ONE
 - Save the Project File as Processor TWO.ACD
 - 7. Download Project File to Processors
 - Download Processor_ONE.ACD file to the processor in the Source / Produced Chassis



- Download Processor_TWO.ACD file to the processor in the Destination / Consumed Chassis as TWO
- Put Processors in RUN Mode
- Verify operation

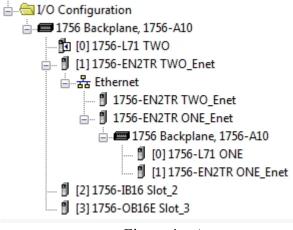


Figure 4 – A

I/O Configuration Processor TWO

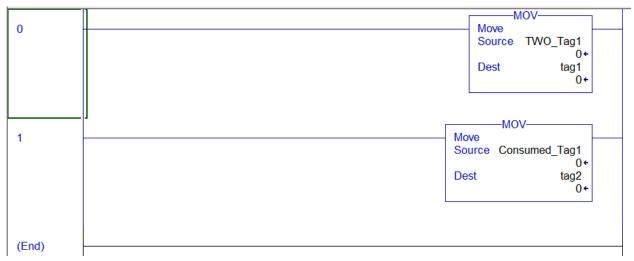


Figure 5 – A Ladder Logic Processor TWO



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