

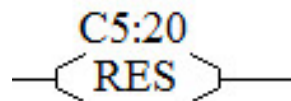
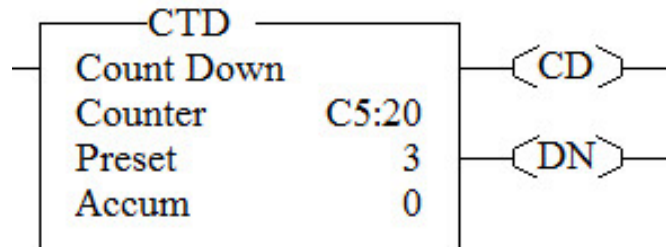
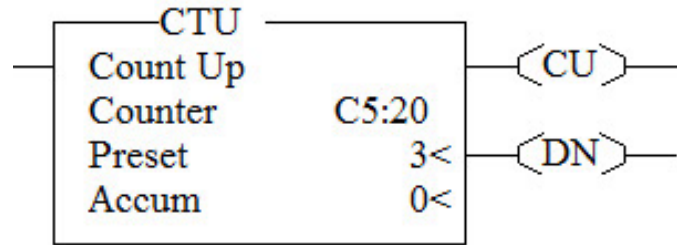
# PLC200

# SLC-500 Counter Instructions

Created by Tom Wylie

On 1/10/16

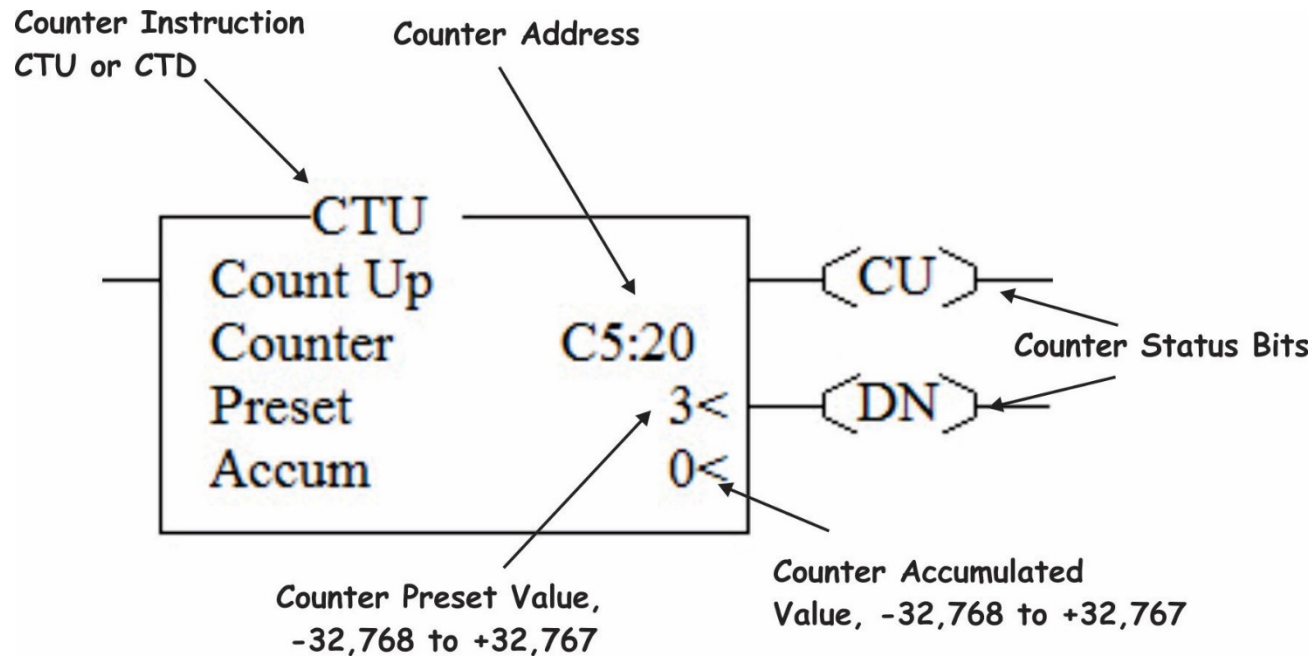
# Allen Bradley Counter Instructions



## Allen Bradley Counters:

- In this lesson the focus will be on 3 counter instructions that are all part of the instruction set of the PLC-5, SLC-500/Micrologix, and the Control/CompactLogix.
- CTU – Count-Up Instruction
- CTD – Count-Down Instruction
- RES – Reset Instruction.
- The data range for counter is signed integer, which is -32,768 to +32767.

# Data in an AB Counter Instruction



**Counter Instruction:** This will be the 3 letter mnemonic, which will be CTU or CTD

**Counter Address:** Each counter must have it's own unique address. If a CTU and CTD are used together, they will have the same address

**Counter Preset:** This is the value the counter must count up to, in meet the planned count.

**Counter Accumulated:** This value will show the currently accumulated counts.

**Counter Status Bits:** These bits show the status of the timer instructions and the data values.

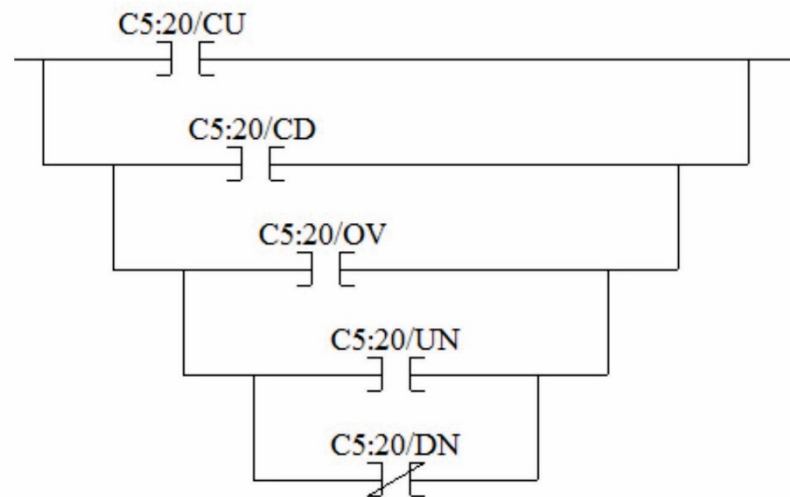
# Counter Status Bits

Offset	CU	CD	DN	OV	UN	UA	PRE	ACC	(Symb)
C5:15	0	0	0	0	0	0	0	0	
C5:16	0	0	0	0	0	0	0	0	
C5:17	0	0	0	0	0	0	0	0	
C5:18	0	0	0	0	0	0	0	0	
C5:19	0	0	0	0	0	0	0	0	
C5:20	1	0	0	0	0	0	3	0	
C5:21	0	0	0	0	0	0	0	0	
C5:22	0	0	0	0	0	0	0	0	
C5:23	0	0	0	0	0	0	0	0	
C5:24	0	0	0	0	0	0	0	0	
C5:25	0	0	0	0	0	0	0	0	
C5:26	0	0	0	0	0	0	0	0	
C5:27	0	0	0	0	0	0	0	0	

Labels above the table with arrows pointing to the CU, CD, DN, OV, UN, and UA columns of row C5:20:

- C5:20/CD
- C5:20/DN
- C5:20/OV
- C5:20/UN
- C5:20/CU

Status bits used in a ladder program



Counter status bits are bits in the counter data file that are set and resets according to the operation of the counter and its data values. Instructions in the ladder program(s) are referenced from these status bits, and will be used to control logic in the program.

The three status bits are:

**.CU** – CTU enable bit.

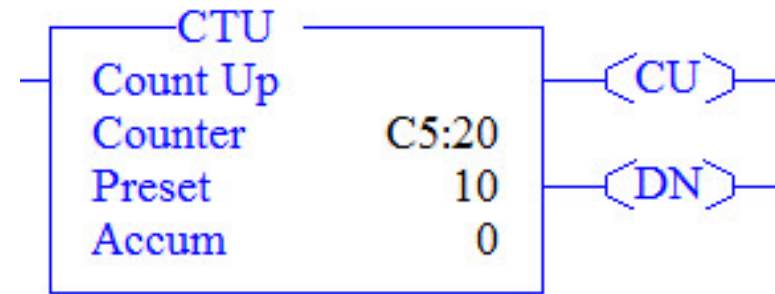
**.CD** – CTD enable bit.

**.DN** – The counter done bit.

**.OV** – The Overflow bit.

**.UN** – The Underflow bit.

# CTU Instruction



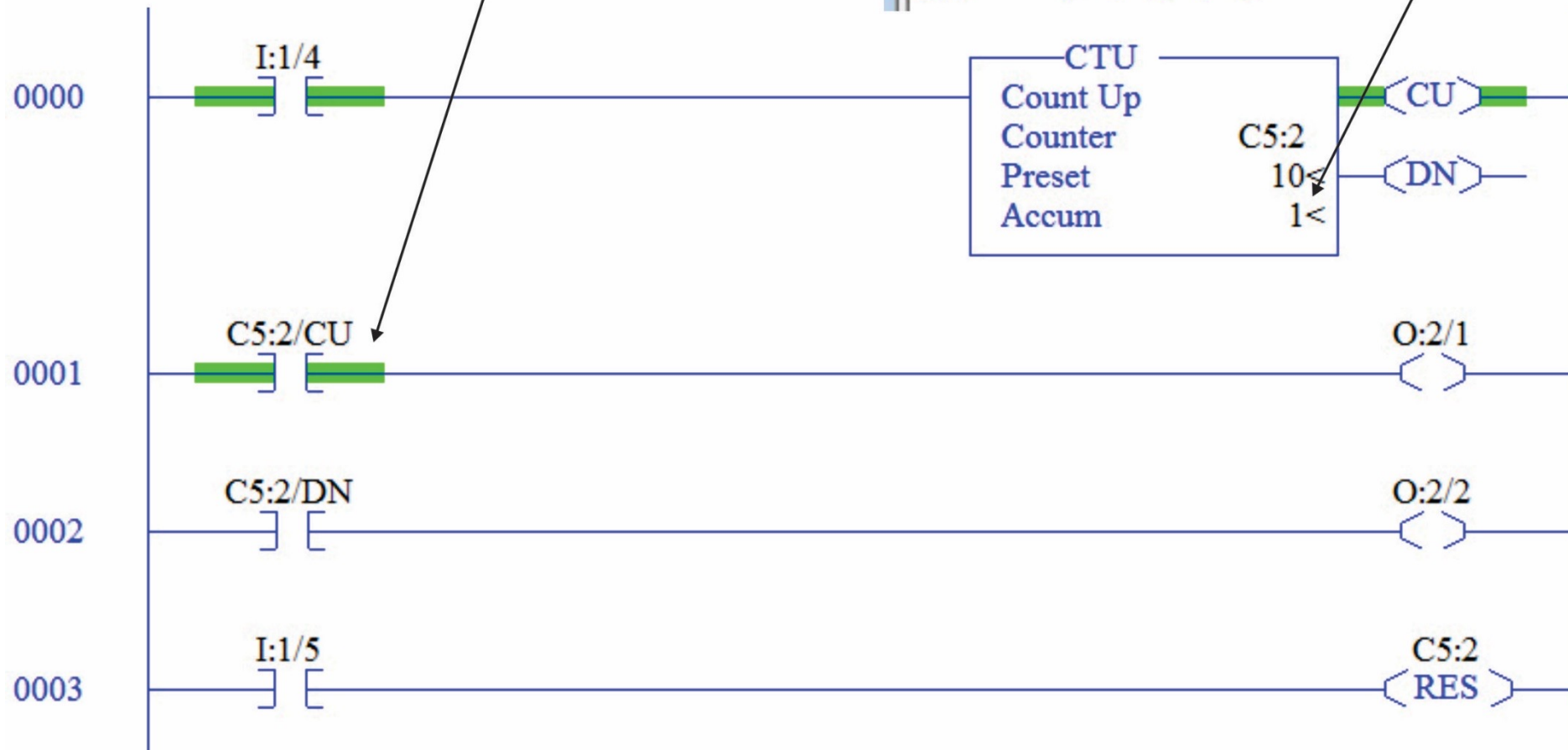
- CTU stands for CounT-Up, which is a count up instruction.
- Every time this instruction is power from an off to on state, the Accumulated value increments by one.
- CTU Status Bits:
  - CU – CTU Enable bit. This bit is on (1) when the CTU instruction is powered.
  - DN – Counter Timer Done bit. This bit is on (1) when the CTU accumulated value is greater than or equal to the preset.
  - OV – Counter Overflow bit. This bit is on (1) when the accumulated value exceeds the maximum counter value (+32,767)
- The Accumulated value will be reset to zero if an RES of the same counter address is energized.

# Example CTU Program

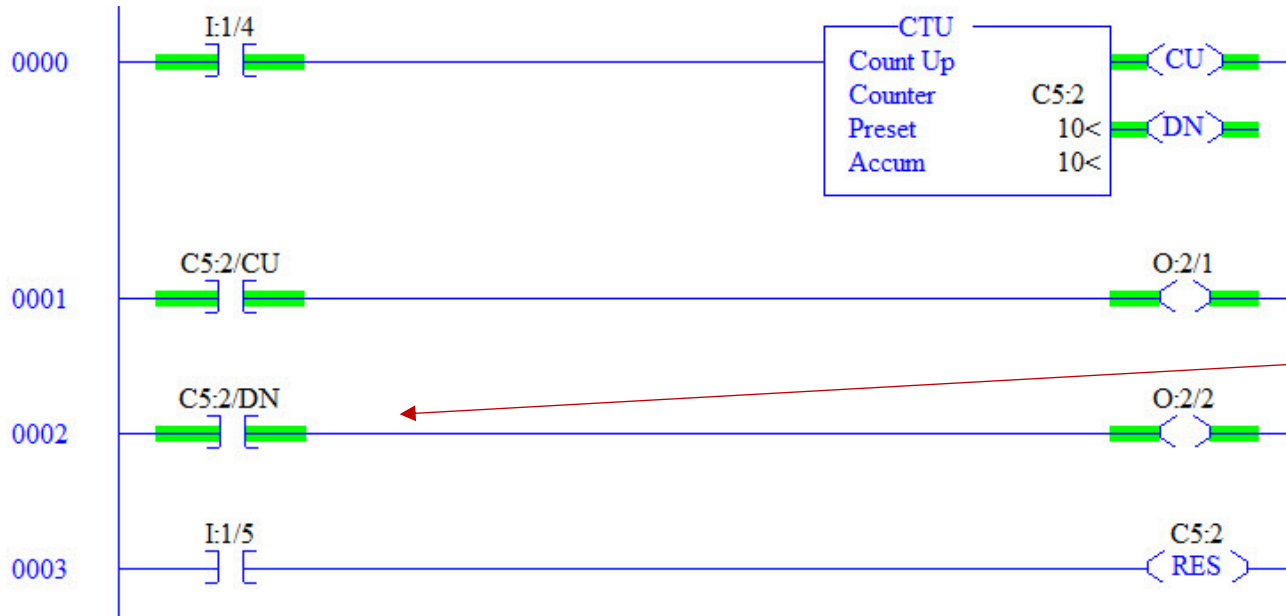
The CTU instruction has power, thus the CTU enable status bit is a "1", which will give power flow to the XIC instruction

Offset	CU	CD	DN	OV	UN
C5:2	1	0	0	0	0

Notice the Accumulated value increments since the CTU was powered.



# Example CTU Program cont.

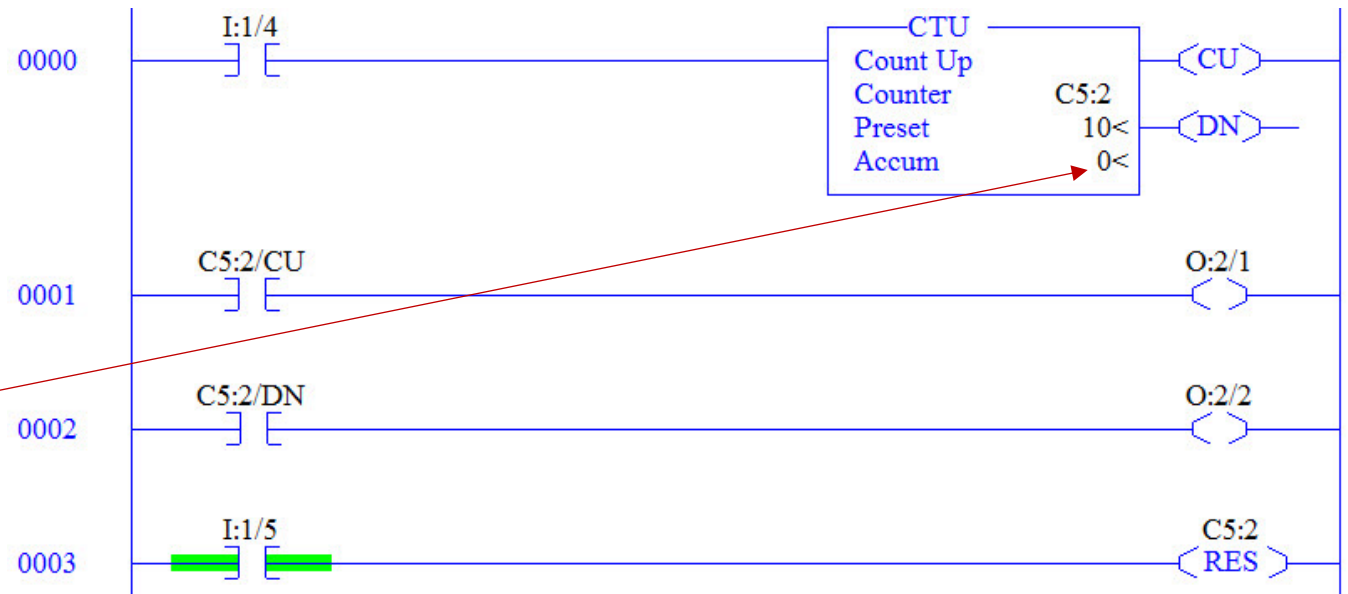


Offset	CU	CD	DN	OV
C5:2	1	0	1	0

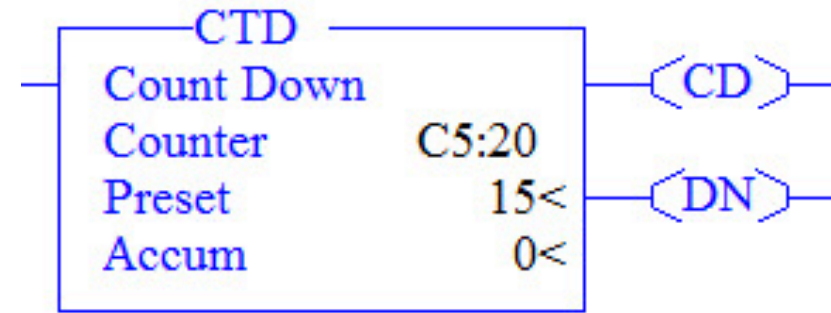
I:1/4 is pulsed 10 times, bringing the Accum value to 10. This turns on the .DN bit.

Offset	CU	CD	DN	OV
C5:2	0	0	0	0

If input I:1/5 is turned on, the Accum value and status bits are reset to zero.



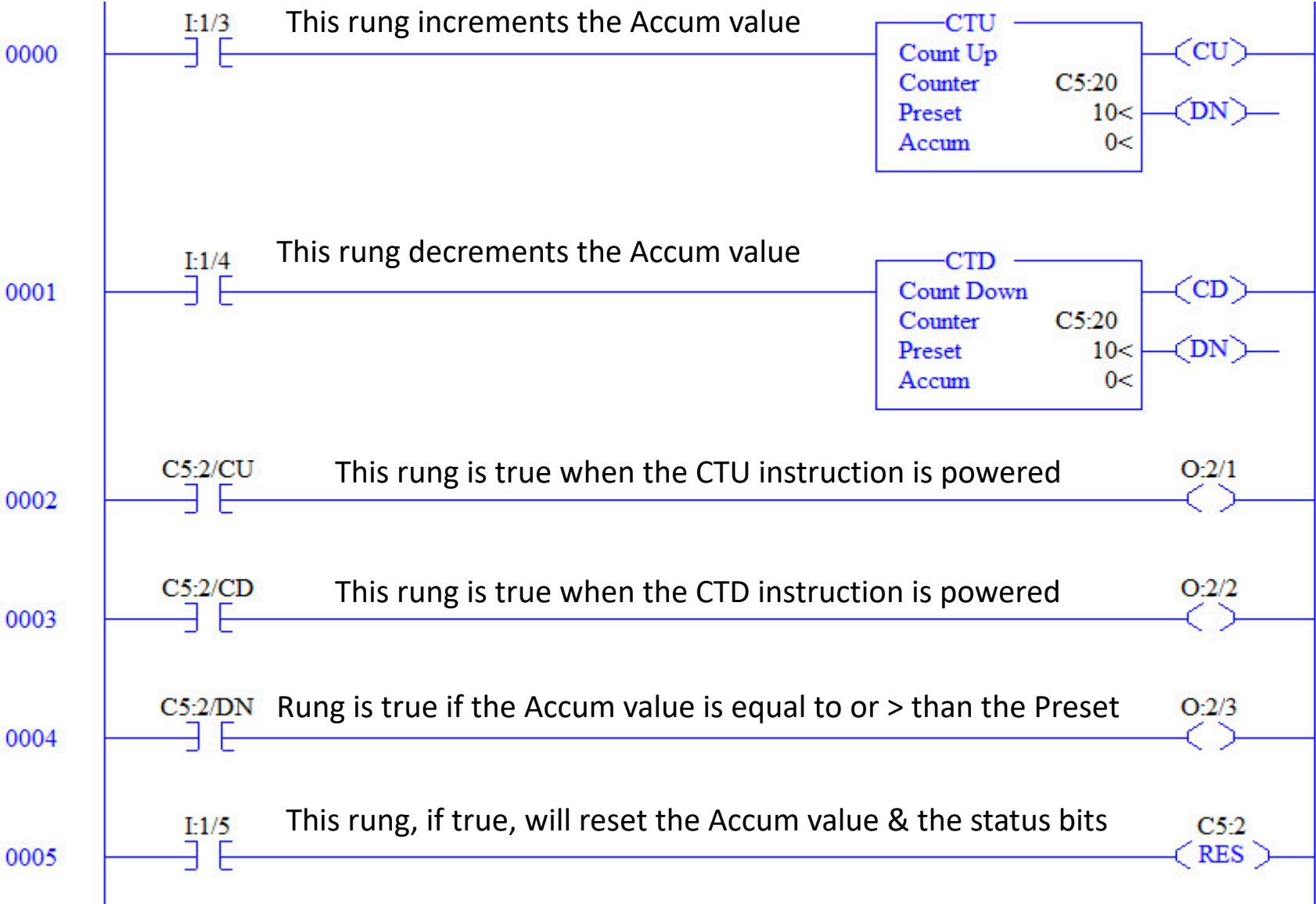
# CTD Instruction



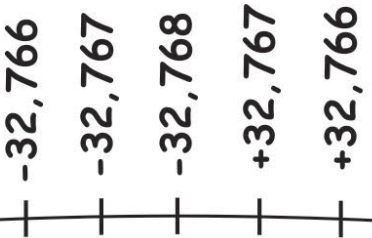
- CTD stands for CounT-Down, which is a count down instruction.
- Every time this instruction is power from an off to on state, the Accumulated value decrements by one.
- CTU Status Bits:
  - CD – CTD Enable bit. This bit is on (1) when the CTD instruction is powered.
  - DN – Counter Timer Done bit. This bit is on (1) when the CTD accumulated value is greater than or equal to the preset.
  - UN – Counter Underflow bit. This bit is on (1) when the accumulated value is at -32,768 and is decremented one more time, which will go past the lowest value.
- The Accumulated value will be reset to zero if an RES of the same counter address is energized.



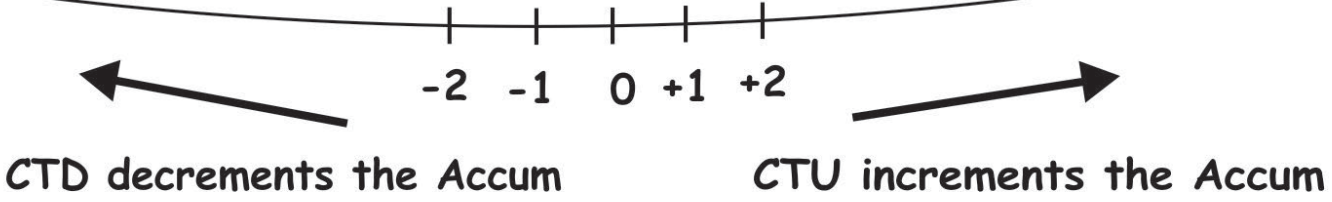
# CTD used with a CTU instruction



# Counter numbering range



The counter numbering range (signed integer) is -32768 to +32767.  
If the CTU increments to +32767, then once more the Accum will be -32768, which will turn on the .OV. If the CTD decrements to -32768, then once more, the Accum will be +32767, which will turn on the .UN bit.

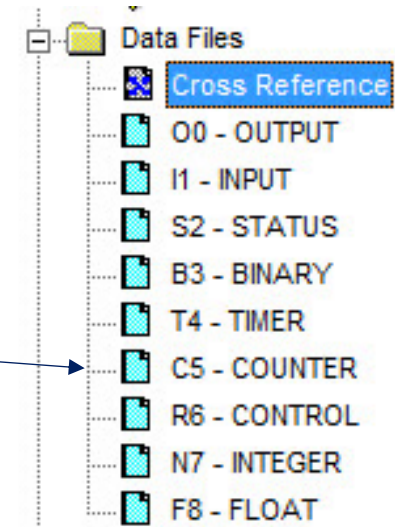


# Counter Addressing

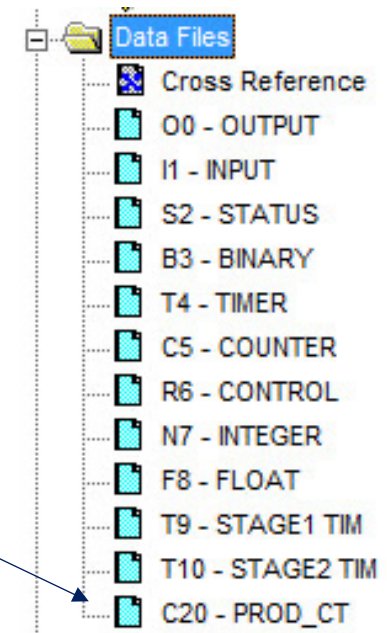
- A counter element is addressed as C5:10.
- A counter element is made up of 3 words:
  - Preset: C5:10.PRE
  - Accum: C5:10.ACC
  - Status bits: C5:10/CU, C5:10/CD, C5:10/DN, C5:10.OV, C5:10/UN
- Each word consists of 16 bits in the preset and accum words.
- Only 3 bits are accessible in the status word
- A user could see bits addressed as: C5:10.ACC/2 (the bit is 0-15)

# Counter Type Data Files

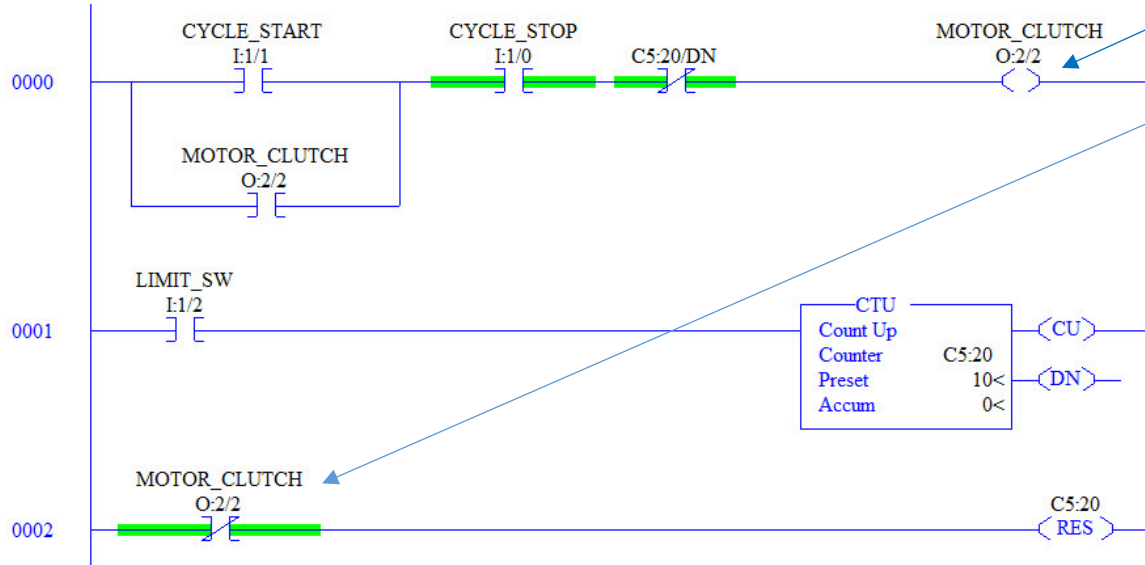
- Data File #5 is a counter file by default.
- Each counter file can have 256 counters (0-255).



- Data files 0-8 are predefined, and files 9-255 can be defined to any type of file except: input, output or status file types.
- In this example, a C20 data file was added. When this file is opened up, the data will be viewed in a counter format

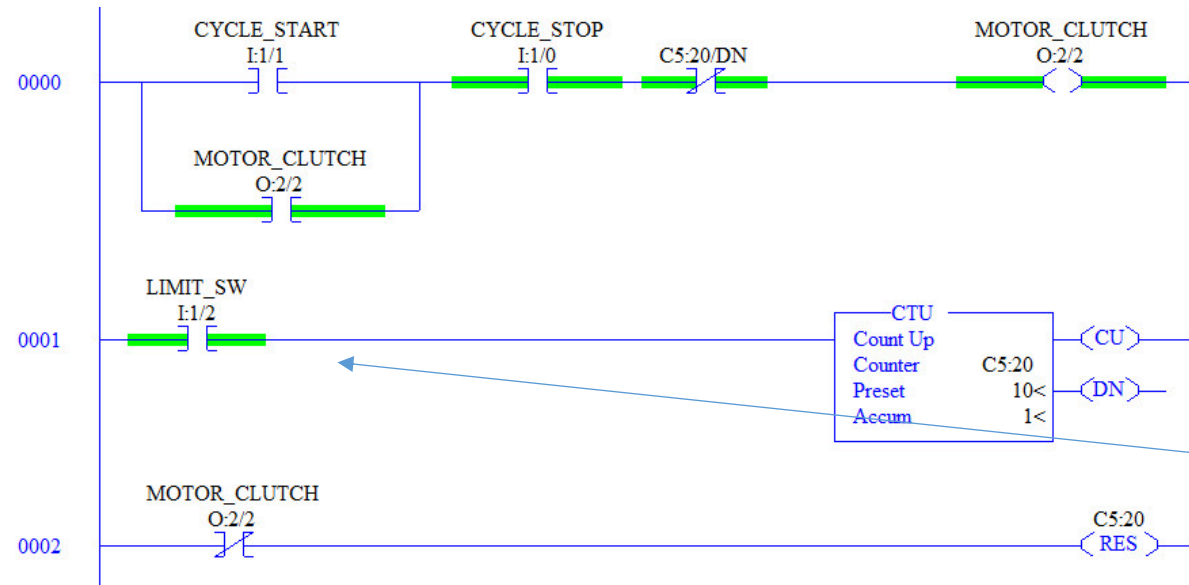
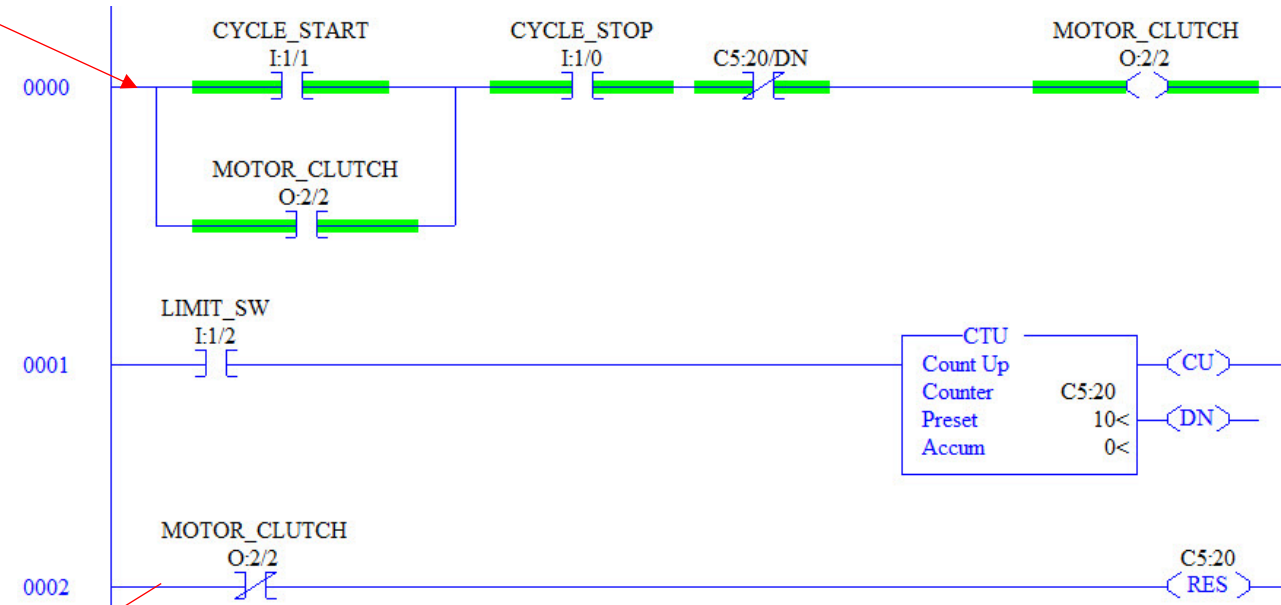


# Example Program



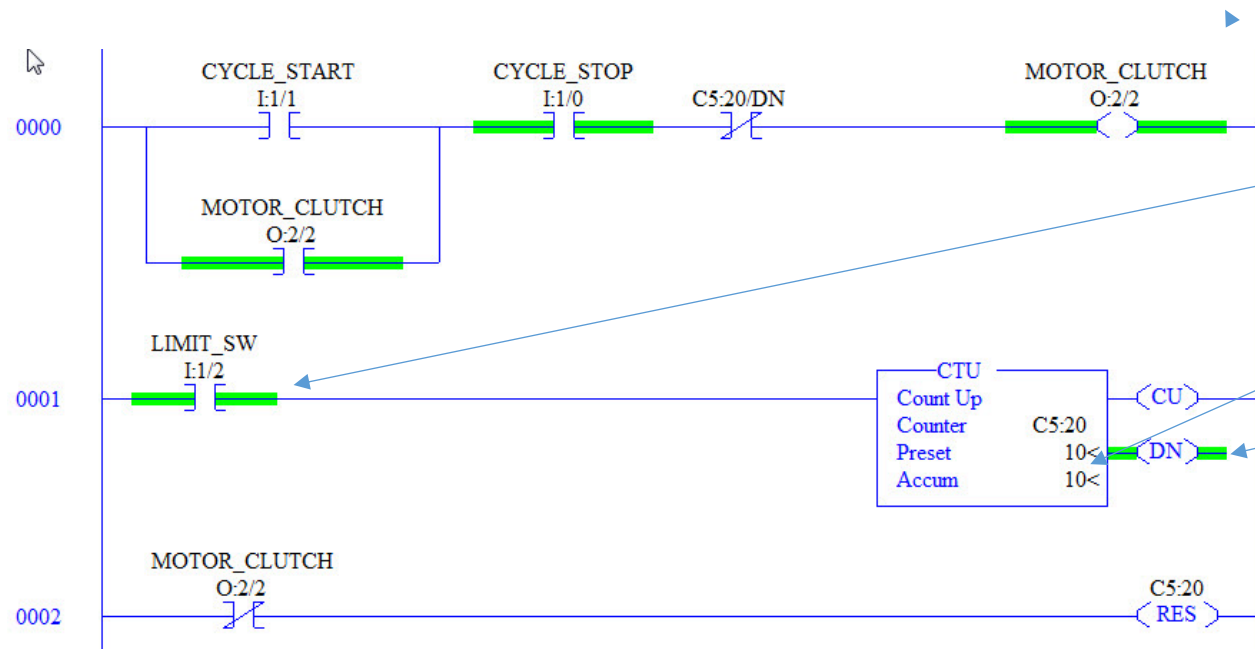
Motor Clutch output is off, which will energize The XIO in rung 002, resetting the Counter.

Cycle\_Start input is momentarily initiated, which energizes the Motor\_Clutch output.



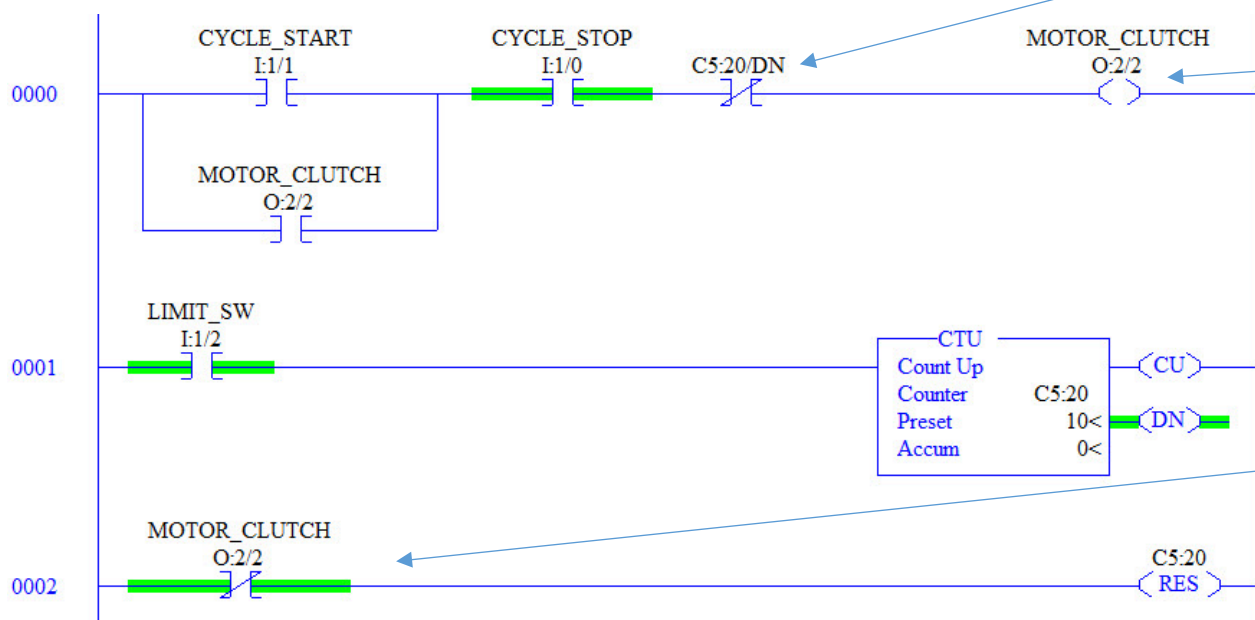
Limit\_Sw is pulsed, which increments the counter

# Example Program cont.



After the Limit\_Sw is pulsed 10 times, the counter Accum value is 10, which turns on the .DN bit

Since the .DN bit is on, the XIO in rung 000 loses highlight (power flow), which drops out the Motor-Clutch output.



When the Motor\_Clutch output is off, the XIO in rung 002 gets highlight, which will power the RES instruction, resetting the Accum value to zero, and resetting the status bit.

# Review Question #1

- The status bit that turns on when a CTU instruction receives power flow is:
  - A. .CU
  - B. .CD
  - C. .EN
  - D. .CE

# Review Question #1 answer

- The status bit that turns on when a CTU instruction receives power flow is:
  - A. .CU**
  - B. .CD
  - C. .EN
  - D. .CE

Explanation:

The .CU or the Count Up Enable bit is turned on when the CTU instruction receives power.



# Review Question #2

- What is the data range for a counter in an SLC-500 based system?
  - A. 0-999
  - B. -999 to +999
  - C. -32,768 to +32,768
  - D. -32,768 to +32,767

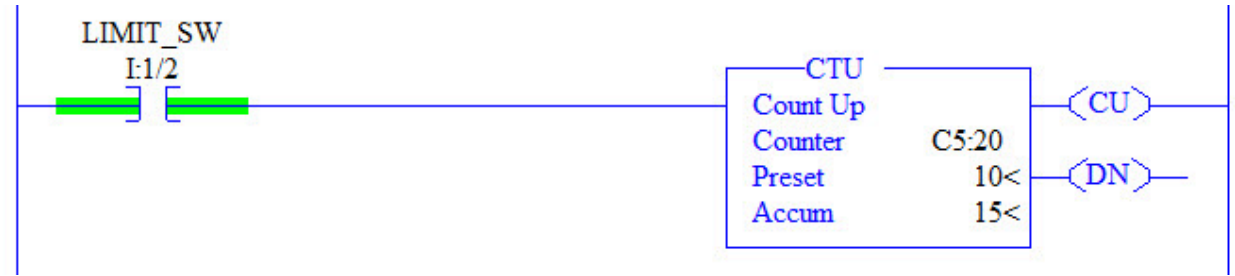
# Review Question #2 answer

- What is the data range for a counter in an SLC-500 based system?
  - A. 0-999
  - B. -999 to +999
  - C. -32,768 to +32,768
  - D. **-32,768 to +32,767**

## Explanation:

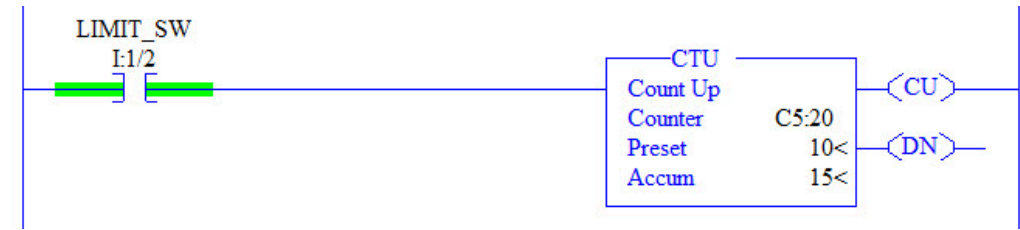
The correct answer is -32,768 to +32,767, which is termed “signed integer”. This is the value stored in a 16 bit word in memory. The counter and integer type of files have this numbering range.

# Review Question #3



- Which counter status bits would be on, based on this rung of logic? (circle all that apply)
  - .CU
  - .CD
  - .DN
  - .OV
  - .UN

# Review Question #3 answer



- Which counter status bits would be on, based on this rung of logic? (circle all that apply)
  - .CU**
  - .CD
  - .DN**
  - .OV
  - .UN

## Explanation:

The .CU (CTU enable bit) is on since the CTU is receiving power flow from the XIC of I:1/2. The .DN bit is also on, since the Accum value is greater than the preset. If the CTU was continually pulsed until it went up to 32767, then pulsed once more, the .OV bit would then come on.

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